Designing Correct Circuits 2008
A Satellite Workshop of ETAPS’08

CALL FOR ABSTRACTS

Budapest, Hungary, 29-30 March 2008

Abstracts due: *** 14 December 2007 ***
Notification of acceptance: 9 January 2008
Final version: 1st February 2008

A two-day workshop on the topic *Designing Correct Circuits* will be held on 29-30 March 2008 in Budapest, as part of the ETAPS group of conferences. The workshop will bring together researchers in formal methods for hardware design and verification from academia and industry. It will allow participants to learn about the current state of the art in formally-based hardware verification and is intended to spark debate about how more effective verification methods can be developed. Much research in hardware verification now takes place in industry, rather than in academia. For the long term survival of our field, we must ensure that academics and industrial researchers continue to work together on the real problems in correct circuit design and verification, including those currently being faced in microprocessor design, System-on-a-Chip development, and in the automotive and aerospace industry.

A major aim of this workshop is to open the necessary communication channels. The DCC workshops have been held on a biennial basis since 2002 and were always a great success in creating an informal forum where these issues were discussed. We hope for something similar in 2008.

This call invites you to submit a one page description of a talk that you would like to give at this workshop. One page abstracts of your talks can be submitted to Gordon J. Pace (gordon.pace@um.edu.mt) by 14 December 2007. The abstract should describe original work, and should indicate what distinguishes your work from other research on languages for and approaches to the design and verification of hardware. Describe the status of your work such as, for example, industrial experience with conclusions, new idea with prototype implementation, new theory, comparison of methods, etc. Please indicate clearly how your talk will contribute to the kind of debate that we are hoping to generate. Include a list of references on a second page if you wish. Researchers from both industry and academia are encouraged to submit talks. Speakers from
industry who would be willing to present research problems that they face (and with which they need help) would also be welcome. We would like to be able to present a broad view of the current state of the art in design and verification methods.

The final programme will be agreed by the workshop committee no later than 9 January 2008, and a final version of the material for the participants proceedings will be due on 1 February 2008. This would preferably be a draft paper, but could also be slides. The workshop speakers and the workshop committee will decide after the workshop whether or not to make a more permanent record, for example by arranging a special issue of a journal.

**Workshop Committee**

Koen Claessen (Chalmers University of Technology, Sweden)
Mike Gordon (University of Cambridge)
Warren Hunt (The University of Texas at Austin)
Samin Ishtiaq (ARM)
Andy Martin (IBM)
Tom Melham (University of Oxford)
John O’Leary (Intel)
Gordon J. Pace (University of Malta)
Tim Sheard (Portland State University)
Mary Sheeran (Chalmers University of Technology, Sweden)
Satnam Singh (Microsoft Research)
Walid Taha (Rice University)

**Web Pages**

The ETAPS08 web page is at [http://etaps08.mit.bme.hu/](http://etaps08.mit.bme.hu/).

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Satnam Singh (satnams@microsoft.com)